www.editada.org

International Journal of Combinatorial Optimization Problems and Informatics, 17(1), Jan-April 2026, 341-354. ISSN: 2007-1558. https://doi.org/10.61467/2007.1558.2026.v17i1.1173

Remote Laboratory Based on FPGA Devices for Education 4.0

Victor H. García Ortega[1,2], Josefina Bárcenas López[1], Enrique Ruiz-Velasco Sánchez[3]
[1]Instituto de Ciencias Aplicadas y Tecnología, Universidad Nacional Autónoma de México, México.
[2]Escuela Superior de Cómputo, Instituto Politécnico Nacional, México.
[3]Instituto de Investigaciones sobre la Universidad y la Educación, Universidad Nacional Autónoma de México, México.

vgarciaortega@comunidad.unam.mx, vgarciao@ipn.mx, josefina.barcenas@icat.unam.mx

Abstract. This paper reports a remote laboratory architecture for Education 4.0 applied to Digital Logic Design courses using FPGA devices. The development of the proposed architecture is based on embedded systems, in which the V-model methodology and an Internet of Things (IoT) technological environment are applied. Nine laboratory exercises were designed for the proposed remote laboratory. To evaluate learners' acceptance of the remote laboratory, the Technology Acceptance Model was used. An evaluation instrument comprising six variables and 21 pre-coded items on a Likert scale was designed and administered to 28 learners via a survey. The Cronbach's alpha coefficients calculated for the six variables ranged from 0.72 to 0.91, suggesting adequate reliability of the evaluation instrument. The Wilcoxon signed-rank test was applied, yielding a p-value below the significance threshold of 0.001, which indicates statistical support for learners' acceptance of the remote laboratory.
Keywords: Education 4.0, remote laboratory, embedded systems, evaluation model.

Article Info
Received July 11, 2025
Accepted August 12, 2025

1 Introduction

The Fourth Industrial Revolution, or Industry 4.0 (I4.0), is a term coined in Germany at the 2011 Hannover Fair to describe how it would revolutionize the organization of global value chains. I4.0 began in the early 21st century and is based on various technologies such as the Internet of Things (IoT), ubiquitous and mobile computing, sensor networks, data science, and artificial intelligence for machine learning. All these fields of knowledge enable the development of innovative technological advancements, leading to a technological revolution that fundamentally changes the way we live, work, and interact with one another (Schwab, 2016).

Education 4.0 (E4.0) has emerged as a result of I4.0, and various researchers have proposed different definitions of the term (Mukul & Büyüközkan, 2023). Some of them include:

E4.0 is described as a movement that fosters non-traditional thinking among learners (Butt et al., 2020).
E4.0 arises from the observation by educational theorists that the Fourth Industrial Revolution will bring a new era to the world and will have a major impact not only on the economy but also on education (Ishak & Mansor, 2020).
E4.0 addresses, on one hand, the use of emerging technologies to enhance the teaching process and, on the other, the approaches and workshops that familiarize young engineers with these technologies, as they will work in Industry 4.0 environments (Mourtzis et al., 2018).
E4.0 responds to society's needs in an era of innovation. It is associated with evolving technologies and their special features such as parallelism, synchronization, and simulation (Puncreobutr, 2016).

E4.0 has been associated with various learning theories and methods related to employment, entrepreneurship, and pedagogy. Some of the theories identified include constructivism and connectivism (Flores et al., 2020).

In constructivist theory, the concept of constructivist teaching and learning is used to designate a position in which various psychological and educational theories converge—such as Jean Piaget's theory—all of which share the assumption that knowledge and learning do not represent a direct copy of reality, but rather an active construction by the individual through interaction with a sociocultural environment (Trilla & García, 2001).

On the other hand, connectivism is the thesis that knowledge consists of sets of connections between entities, such that a change in one entity can result in a change in another, and that learning is the growth, development, modification, or strengthening of those connections (Downes, 2022). Connectivism integrates principles explored by the theories of chaos, networks, complexity, and self-organization (Siemens, 2004).

E4.0, as a new educational approach, promotes not only the use of digital technologies, but also the development of applications to improve teaching and learning processes in courses taught at different educational levels. One of the key activities carried out by learners across different courses is the development of practical sessions, which help consolidate the knowledge and learning of theoretical content covered in class. This type of activity is undoubtedly constructivist in nature, as it is traditionally conducted in physical laboratories within academic institutions. However, on-site laboratories present several challenges, which are outlined below:

1. It is not possible to use physical laboratories during the suspension of academic activities due to unforeseen events, such as the COVID-19 pandemic. According to the United Nations (2023), this health emergency caused learning delays in four out of five of the 104 countries studied. Additionally, lab maintenance, labor or learner strikes, among other issues, also hinder access to physical labs.

2. Even during regular academic periods, access time to physical laboratories is very limited and often does not meet the needs of the various courses in the curricula of upper secondary and higher education programs. Typically, each course is allocated only one lab session per week, which is insufficient for theory-practice integration.

3. Among the United Nations' Sustainable Development Goals (SDGs), SDG 4 seeks to "ensure inclusive, equitable, and quality education and promote lifelong learning opportunities for all" (United Nations, 2018). This goal includes guaranteeing learning and development in science and technology for learners at all educational levels and across disciplines. In Mexico, the development of microsystems using Field Programmable Gate Array (FPGA) technology has been promoted since 2007 (FUMEC, 2022), as it is a key area for technological innovation. However, many degree programs lack access to this technology in their institutional laboratories.

4. The digital divide refers to the disparity in access to, skills in, and use of ICTs among individuals, organizations, regions, and countries (Van Dijk & Jan, 2020). In 2024, telephone (landline or mobile) access in Mexican households rose to 96.1%, while computer usage increased to 43.9% among individuals aged six and older (INEGI, 2024). Additionally, the number of Internet users in Mexico reached 101.9 million, representing 84% of the population aged six and older (Asociación de Internet MX, 2024). Despite this increase in the use of computers, telephony, and Internet access, a significant gap remains in the meaningful appropriation of technology in Mexico—particularly in its application within educational laboratories.

As an alternative solution within the framework of E4.0, Remote Laboratories (RLs) emerge as disruptive technological environments for conducting practical sessions at a distance. Through RLs, it is possible to propose innovative technological models that address the previously mentioned challenges.

These types of laboratories are computational systems that allow remote interaction with the physical equipment located in the laboratories of academic institutions at any educational level. The RL provides the entire infrastructure required for learners to test their lab exercises from anywhere—such as home, school, or work. This infrastructure includes servers for uploading files to the physical equipment, applications for interacting with the hardware, video streaming to observe the results of the experiments, and, of course, a network connection for Internet access. This infrastructure enables RLs to operate within the technological environment known as the IoT (Kramp et al., 2013; Kumar, 2019; Milenkovic, 2020; Vargas & Durá, 2014).

This technological environment allows everyday objects to be connected to the Internet and to receive, generate, and transmit data without human intervention. IoT applications are developed using embedded systems, which are computational systems designed with dedicated hardware and software—using digital technologies—to perform specific tasks, thereby offering advantages in performance, cost, and system usability.

In particular, RLs can be developed with embedded systems that operate with high efficiency and very low cost. It is within these types of technological environments that connectivism becomes relevant, through the various teaching and learning activities that are carried out.

RLs have been developed for various areas, such as control systems (Chevalier et al., 2016) and programming education (Álvarez Ariza & Gil, 2022). Another important area of RL development is Digital Logic Design, where FPGA devices are used for application implementation (Navas et al., 2023; Fujieda & Okuchi, 2023; Melosik et al., 2022).

This article presents the development of a technological model through a RL using reconfigurable FPGA technology for Digital Logic Design courses. The technological model is implemented using embedded systems and the IoT technological environment, offering a proposed solution to the challenges faced in traditional physical laboratories. The submitted proposal is evaluated using the Technology Acceptance Model (TAM) through descriptive and inferential statistics.

2 Experimental procedures

2.1 Technological model of the remote laboratory

The proposed technological model is shown in Figure 1 and consists of two main components:

- **Remote Laboratory based on IoT**. The RL is implemented using embedded systems with System-on-Chip (SoC) technology, based on the Linux operating system. These types of technological environments are custom-designed depending on the specific area in which they are to be implemented.

- **Learning Management System (LMS).** The LMS contains the course content, which includes lecture notes, learning activities, and lab exercises.

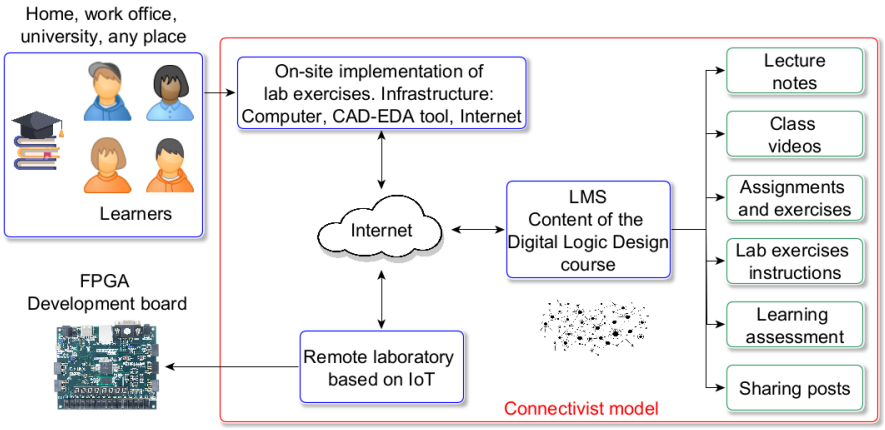

Fig. 1. Proposed technological model.

2.2 V-model methodology for embedded systems

For the analysis, design, and implementation of the RL using an embedded system, an adaptation of the V-model methodology proposed by Coop (2006) was used for the development of SoC-based embedded systems. This methodology is shown in Figure 2.

Figure 2 shows the stages of the V-model methodology, from the specification of requirements to the operational testing of the system. This methodology allows returning to previous stages to make the necessary adjustments and ensure that the established requirements are met. In addition, the methodology supports the use of Unified Modeling Language (UML) in each stage (Booch et al., 1999), enabling a detailed description and a standardized design.

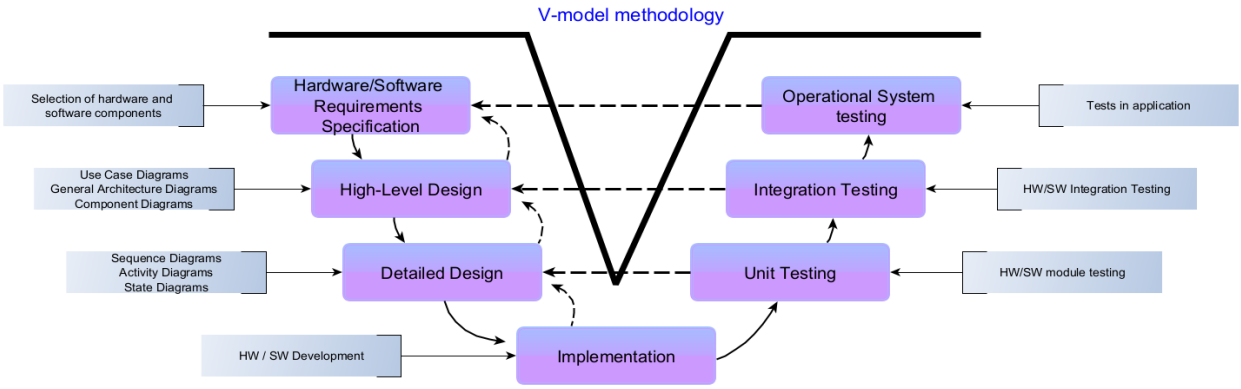

Fig. 2. V-model methodology for embedded systems.

2.3 Remote laboratory architecture

As a result of applying the V-model methodology, the RL presented in this article was implemented. It is focused on the area of Digital Logic Design using a Nexys 4 development board (Digilent, 2025), which is based on the XC7A100T FPGA from the Artix-7 family by Xilinx (2025).

The RL uses a Camera Module V2 for Raspberry Pi (2025a), which features Sony's IMX219 8-megapixel sensor (2025) for live video streaming. This camera communicates with the SoC via the MIPI CSI-2 protocol (MIPI Alliance, 2025). Additionally, the RL includes a manipulation interface that connects the SoC's GPIOs to the Nexys 4 development board, creating a connector referred to as "LAB REMOTO", which supports the operation of up to 24 virtual switches.

For the implementation of the RL, a Raspberry Pi 4 Model B SoC with 1 GB of RAM was selected. This board uses a Broadcom BCM2711 chip featuring a 64-bit quad-core ARM Cortex-A72 processor (Raspberry Pi, 2024b). The operating system used is Raspberry Pi OS Lite (64-bit), which has an image size of 438 MB (Raspberry Pi, 2024c). Figure 3 shows the architecture of the FPGA-based Remote Laboratory.

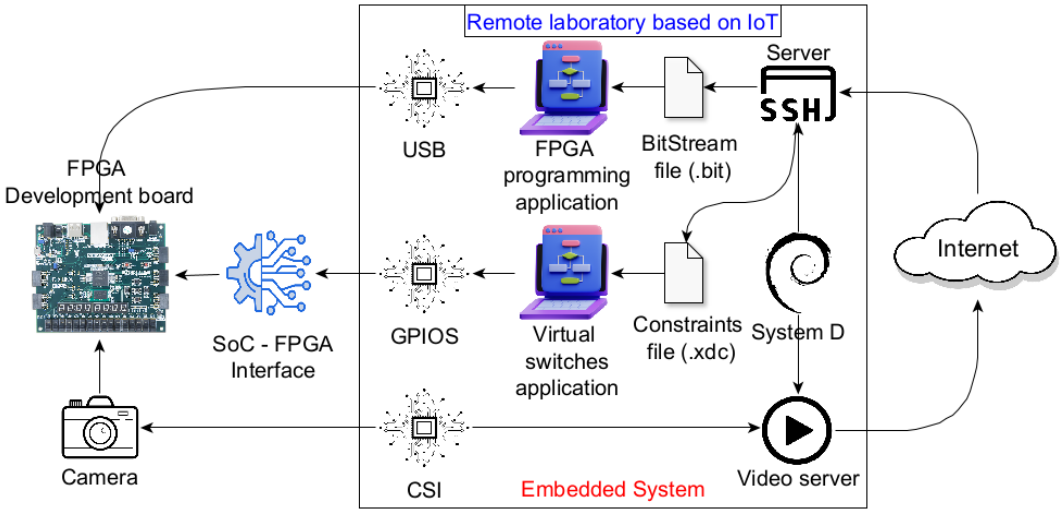

Fig. 3. Remote laboratory architecture.

Figure 3 shows the execution of an SSH server, which enables remote access and file transfer to the laboratory. The actions carried out through this server are as follows:

- **Transfer of the binary (.bit) file.** This file is generated using the ISE or Vivado development tools (AMD, 2025) at the location where the learner is working. It contains the design of the lab exercise and is used to program the FPGA.

The programming is performed via an application that uses Joint Test Action Group (JTAG) drivers for the ARM architecture.

- **Transfer of the constraint (.xdc) file.** This file contains the terminal assignments and the signal names for the inputs and outputs of the lab exercise. The input terminals are assigned to virtual switches through the LAB REMOTO connector.
- **Remote access to the laboratory.** Access is granted from any device with an SSH client application. On the SoC, an application is used to interact with, test, and verify the lab exercise on the FPGA.

In addition, a video server is used to visualize the results of the lab exercise through live video streaming.

2.4 Learning Management System

The LMS contains the content of the Digital Logic Design course, which includes: lecture notes, assignments and exercises, class videos, instructional design documents for the lab exercises, shared posts, learning assessment activities, and lab exercise reports.

Nine lab exercises, that cover the complete course, were implemented in the RL. These lab exercises are shown in table 1.

Table 1. Lab exercises of the Digital Logic Design course

No	Lab exercise title	Course topic
1	Combinational logic	Introduction
2	Flip-Flops	Latches and Flip-Flops circuits
3	Registers	Registers: architectures and applications
4	Sequence detector	Register applications, Mealy Machine
5	Multiplexed message	Moore Machine
6	Counters	Counters: architectures and applications
7	Special counters	BCD, Ring and Johnson counters
8	Sensors	Mealy Machine, special counters applications
9	Algorithmic State Machines (ASM)	Registers, counters and memories applications, ASM

Each of the lab exercises shown in Table 1 is described below:

The first lab exercise involves integrating different combinational logic circuit elements such as multiplexers, comparators, and code converters into a single application. This allows the use of various VHDL structures (IEEE, 2019), including concurrent, sequential, and conditional statements. In this lab exercise, learners review and/or acquire the foundational knowledge required for the course.

In the second lab exercise, learners design, implement, and test SR, JK, T, and D flip-flops based on equations derived from their extended truth tables. The implementation is carried out using D flip-flops and VHDL on an FPGA. Through this lab exercise, learners apply and reinforce their theoretical knowledge of latches and flip-flops circuits.

In the third lab exercise, learners design, implement, and test a circuit that performs the functions of a register, including load, hold, shift-left, and shift-right operations. The implementation is carried out at different abstraction levels using VHDL on an FPGA. In this lab, learners apply and reinforce their understanding of register architectures and their applications.

In lab exercise 4, learners design, implement, and test a 4-bit overlapping sequence detector using VHDL on an FPGA. The sequence to be detected is ***1101***, applying the sequential design methodology. In this lab, learners apply and reinforce their knowledge of Deterministic Finite Automata (DFA) with outputs, specifically Mealy Machines.

In lab exercise 5, learners design, implement, and test a multiplexed message using VHDL on an FPGA. The message consists of four symbols displayed on a four-digit common-anode seven-segment multiplexed display. Sequential design methodology is also applied. The implementation includes two versions: a static message and a scrolling marquee-style message. In this lab, learners apply and reinforce their knowledge of DFAs with outputs, specifically Moore Machines.

In lab exercise 6, learners design, implement, and test counters using VHDL on an FPGA. They analyze an up-counter with enable signal to derive a generic equation using a Moore Machine and apply sequential design methodology. Counters are also implemented using high-level operators + and -. This lab allows learners to apply and reinforce their knowledge of counters.

In lab exercise 7, learners design, implement, and test BCD, ring, and Johnson counters using VHDL on an FPGA. These counters are analyzed using Mealy and Moore Machines and are implemented using packages and components. This lab allows learners to apply and reinforce their knowledge of special-purpose counters.

In lab exercise 8, learners design, implement, and test an application that detects whether a person enters or exits a room and counts the number of people inside using two optical sensors and BCD counters. The application is designed using a Mealy Machine, with states and transitions implemented using high-level VHDL statements. Packages and components are used in the implementation. Through this lab, learners reinforce their understanding of Mealy Machines and special-purpose counters.

In lab exercise 9, learners design, implement, and test an application that determines the number of logic "1" bits in a 22-bit register. The application is designed using an ASM, where packages and components are used for implementation through VHDL statements on an FPGA. In this lab, learners apply and reinforce their knowledge of ASMs.

3 Results and discussion

The proposed technological environment is evaluated using different statistical measures, as shown in Figure 4.

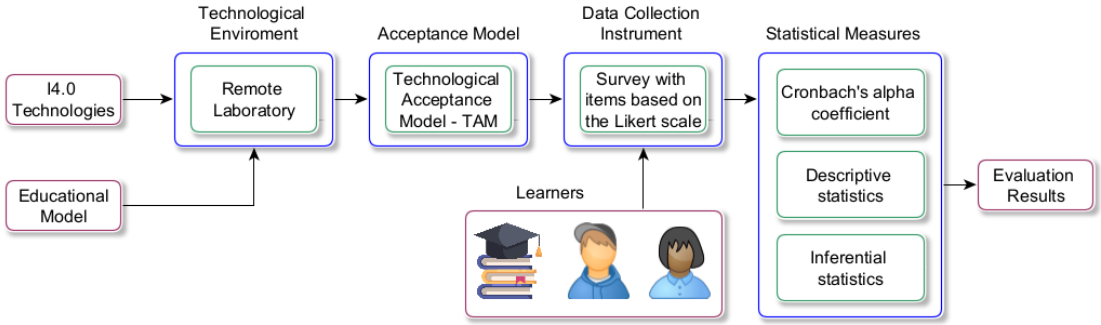

Fig. 4. Evaluation Model.

3.1 Evaluation using the Technological Acceptance Model

The RL is evaluated using a quasi-experimental design through a survey conducted with a group from the Digital Systems Design course at the Escuela Superior de Cómputo (ESCOM), part of the Instituto Politécnico Nacional (IPN). The survey applies the TAM, a theoretical framework developed by Fred Davis (1989) in the 1980s to understand and predict user acceptance and adoption of technology.

The model includes the following variables:

- **Perceived Usefulness (PU):** Defined as the degree to which a person believes that using a particular system would enhance their job performance.
- **Perceived Ease of Use (PEU):** Refers to the degree to which a person believes that using a particular system would be free of effort.
- **Intention to Use (IU):** Refers to the degree to which a person intends to continue using a particular system.

In addition to the PU, PEU, and IU variables, three additional variables are proposed:

- **Technology Application (TA):** Refers to the degree to which a person applies foundational knowledge from technology-related fields when using the system.
- **Support Digital Resources (SDR):** Refers to the digital resources available to the user for operating and managing the technology.
- **Acquired Digital Skills (ADS):** Refers to the knowledge gained through learning the digital technologies required to use a particular system.

The adapted TAM for evaluating the proposed RL is shown in Figure 4.

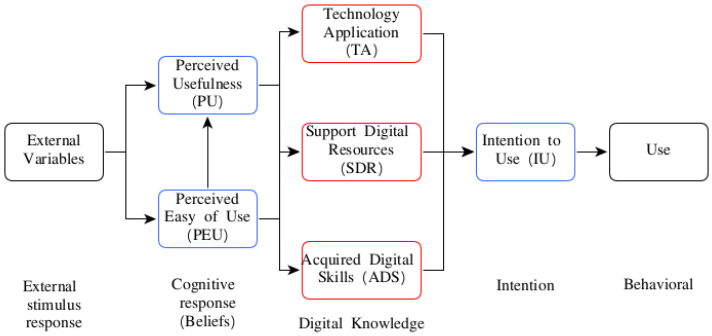

Fig. 5. The adapted TAM.

Figure 3 shows the different variables of the adapted TAM, which were used to design a data collection instrument consisting of a 21-item survey, as shown in Table 2.

Table 2. Survey items corresponding to each TAM variable

Variable	Tag	Items
Learner profile	LP1	Age
	LP2	Gender
PU	PU1	The RL allows learners for performing lab exercises remotely in an innovative way.
	PU2	The RL allows learners to gain practical knowledge of the topics covered in the course.
	PU3	The RL access can be done from anywhere and at any time.
	PU4	The use of the RL allowed me to self-organize with my team members to experiment and learn.
PEU	PEU1	The application for programming the BitStream file onto the FPGA is easy to use.
	PEU2	The application for interacting with the RL connector allows for easy input value assignment to test the lab exercises.
	PEU3	The video server allows the visualization of the lab exercise results.
	PEU4	The live video stream allows the results of the lab exercises to be viewed clearly and sharply.
	PEU5	Assigning terminals on the REMOTE LAB connector using the constraints file is easy to do.
TA	TA1	The use of the RL allows learners to acquire and apply knowledge from the Computer Networks course.
	TA2	The use of the RL allows learners to acquire and apply knowledge from the Operating Systems course.
SDR	SDR1	The educational materials (theoretical documents, assignments, and lab exercises) available on the Moodle platform support the learning of the course topics.
	SDR2	The educational resources available on the Moodle platform assist in managing the RL.
	SDR3	The visual and interactive designs of the microarchitectures for each lab exercise facilitate their programming.
ADS	ADS1	The use of the RL allowed me to use different devices, such as mobile devices, desktop computers (PCs), and laptops to experiment with the lab exercises.
	ADS2	The use of the RL enabled me to use applications (Termux, Termius) on a mobile device to experiment with the lab exercises.
	ADS3	The Vivado development tool allowed me to develop HDL programs, perform simulations, assign I/O terminals, and generate the binary (.bit) file for each lab exercise in the course.
IU	IU1	Would you like to continue using the RL in future courses, such as Computer Architecture, elective courses, among others?
	IU2	Would you like to continue using the RL for the development and learning of academic and personal projects?

The items shown in Table 3 were applied during the 2024-2 semester to 28 learners from group 4CV4 of the Digital Systems Design course, using the B-Learning approach (Núñez-Barriopedro et al., 2019), through a self-administered survey with pre-coded items based on the Likert scale.

The Likert scale consists of the following values: strongly agree (SA), agree (A), neutral (N), disagree (D), and strongly disagree (SD). Regarding item LP1, the surveyed learners are between 19 and 23 years old, with most of them (46.4%) being 20 years old. Regarding item LP2, 85.7% of the learners are male and 14.3% female. The results obtained from the remaining items are shown in Table 3.

Table 3. Results of the survey applied

Variable	Tag	(D)	(N)	(A)	(SA)	Variable	Tag	(D)	(N)	(A)	(SA)
PU	PU1		7.1%	7.1%	85.7%	TA	TA1		14.3%	39.3%	46.4%
	PU2		3.6%	14.3%	82.1%		TA2	3.6%	14.3%	46.4%	35.7%
	PU3			21.4%	78.6%	SDR	SDR1			25%	75%
	PU4	3.6%	28.6%	7.1%	60.7%		SDR2			28.6%	71.4%
PEU	PEU1		10.7%	14.3%	75%		SDR3			10.7%	89.3%
	PEU2	3.6%	7.1%	14.3%	75%	ADS	ADS1		3.6%	10.7%	85.7%
	PEU3			14.3%	85.7%		ADS2		3.6%		96.4%
	PEU4		10.7%	25%	64.3%		ADS3		3.6%	10.7%	85.7%
	PEU5	3.6%	7.1%	28.6%	60.7%	IU	IU1		3.6%	7.1%	89.3%
							IU2		3.6%	7.1%	89.3%

Table 3 shows the results for the different variables. Regarding the items of the PU variable, the combined percentage of the (SA) and (A) responses ranges between 67.8% and 100%, indicating that the RL supports the completion of Digital Logic Design lab exercises.

For the PEU variable, the combined percentage of (SA) and (A) responses ranges from 89.3% to 100%, indicating that the applications developed on the SoC allow effective interaction and manipulation of the RL through the FPGA-based development board.

For the TA variable, the combined (SA) and (A) responses range from 82.1% to 85.7%, suggesting that knowledge acquired in other courses is applied and/or learned in the use of the RL.

For the SDR variable, the combined percentage of (SA) and (A) responses is 100%, indicating that the support materials provided follow an appropriate techno-pedagogical design for using the RL.

For the ADS variable, the combined (SA) and (A) percentage is 96.4%, indicating that various computing devices were used to operate the RL and that learners learned to use the Xilinx CAD-EDA tool.

For the IU variable, the combined (SA) and (A) percentage is 96.4%, suggesting that learners would use the RL in future courses or academic projects.

These results demonstrate a very high level of acceptance among learners for the use of the RL. Additionally, learners provided open-ended comments in the survey. Some of them include:

- **Learner 1:** "It is an excellent tool for learners who are learning about the use of technologies such as FPGAs with VHDL."
- **Learner 2:** "It was very practical, from the fact that it was available at night to the benefit of not needing to buy an FPGA. Also, learning about FPGAs was great. I loved the remote lab and would really like to continue using it because of how practical and easy it is to use directly on the server."

- **Learner 3:** "It is very practical, because when working in teams, sometimes we can only use the lab when physically present or, if we only have one board, only one teammate can work at a time. With the remote lab, we can access and view the lab from anywhere without needing to be in the same location."

3.2 Cronbach's alpha coefficient

To determine the reliability of the data collection instrument, Cronbach's Alpha Coefficient was used (Cronbach, 1951; Oviedo & Campo-Arias, 2005; Streiner, 2003), which is obtained by calculating the variances of the responses given by each sample for each item. The equation is given by:

$$\alpha = \frac{k}{(k-1)}\left(1 - \frac{\sum_{i=1}^{k} \sigma_i^2}{\sigma_T^2}\right) \quad (1)$$

The Cronbach's Alpha Coefficient was calculated for each of the TAM variables and for all the items in the survey. This was done using a program developed with the Pandas library (2025) and the Jupyter Notebook development environment (Jupyter, 2025). The values obtained are shown in Table 4. The values obtained are shown in Table 4.

Table 4. Values of the Cronbach's Alpha Coefficient

Variable	Cronbach's Alpha Coefficient
PU	0.729
PEU	0.738
TA	0.762
SDR	0.780
ADS	0.910
IU	0.774
PU, PEU, TA, SDR, ADS, IU	0.866

The values obtained for the variables range from 0.729 to 0.91, indicating that the data collection instrument has good internal consistency of the items within each variable.

3.3 Application of descriptive statistics

To perform the analysis and interpretation of the results obtained for each TAM variable, descriptive statistics were used. The sample mean ($\bar{x}$) was calculated as a measure of central tendency. In addition, the sample variance (s^2), standard deviation (s), and coefficient of variation ($CV = s/\bar{x}$) were calculated as measures of dispersion. This was done using a program developed with the Pandas library (2025) and the Jupyter Notebook development environment (Jupyter, 2025).

Table 5. Measures of central tendency and dispersion

Items	$\bar{x}$	s^2	s	$CV(\%)$	Variables	$\bar{x}$	s^2	s	$CV(\%)$
PU1	4.78	0.32	0.56	11					
PU2	4.78	0.24	0.49	10	PU	4.65	0.48	0.69	14
PU3	4.78	0.17	0.41	8					
PU4	4.25	1	1	23					
PEU1	4.64	0.46	0.67	14					
PEU2	4.60	0.61	0.78	17					
PEU3	4.85	0.12	0.35	7	PEU	4.62	0.46	0.68	14
PEU4	4.53	0.48	0.69	15					
PEU5	4.46	0.62	0.79	17					
TA1	4.32	0.52	0.72	16	TA	4.23	0.58	0.76	18
TA2	4.14	0.64	0.80	19					
SDR1	4.75	0.19	0.44	9					
SDR2	4.71	0.21	0.46	9	SDR	4.78	0.17	0.41	8
SDR3	4.89	0.09	0.31	6					
ADS1	4.82	0.22	0.47	9					

ADS2	4.92	0.14	0.37	7	ADS	4.85	0.19	0.44	9
ADS3	4.82	0.22	0.47	9					
IU1	4.85	0.20	0.44	9	IU	4.85	0.19	0.44	9
IU2	4.85	0.20	0.44	9					

The sample mean ($\bar{x}$) values obtained for the variables PU, PEU, TA, SDR, ADS, and IU range from 4.14 to 4.92, indicating a high positive perception of the RL by the learners. Additionally, the coefficient of variation (*CV*) for the items shows values ranging from 6% to 23%, indicating that the data dispersion is low relative to the sample mean ($\bar{x}$). Since the variables SDR, ADS, and IU have a *CV* below 10%, they show high homogeneity. The variables PU, PEU, and TA have a *CV* below 20%, indicating moderate homogeneity (Brown, 1998; Jalilibal et al., 2021).

3.3 Application of inferential statistics

To obtain statistical evidence of learners' perception and acceptance of the RL, non-parametric statistics were used, since the original distribution of the data cannot be determined (Rios et al., 2020). For this purpose, a statistical normality test was performed to determine whether the data from the applied survey follow a normal distribution. Given the sample size of 28 learners, the Shapiro–Wilk test was used (Shapiro & Wilk, 1965), where the test statistic *W* is given by:

$$W = \frac{(\sum_{i=1}^{n} a_i x_i)^2}{\sum_{i=1}^{n}(x_i - \bar{x})^2} \quad (2)$$

Its test hypotheses are:

H_o: The data follow a normal distribution
H_a: The data do not follow a normal distribution

The *W* statistic was obtained using the statistical library of the Scipy Application Programming Interface (API) (Gommers et al., 2024), within the Jupyter Notebook development environment (Jupyter, 2025). The significance value used is α = 0.001. Table 6 shows the results of the W statistic for each item in the survey.

Table 6. Results of the Shapiro-Wilk test

Items	p-value	*W* test statistic	Conclusion (p < 0.001)
PU1	0.000000	0.427312	H_o is rejected and H_a is accepted
PU2	0.000000	0.489032	H_o is rejected and H_a is accepted
PU3	0.000000	0.507680	H_o is rejected and H_a is accepted
PU4	0.000003	0.698541	H_o is rejected and H_a is accepted
PEU1	0.000000	0.572716	H_o is rejected and H_a is accepted
PEU2	0.000000	0.573988	H_o is rejected and H_a is accepted
PEU3	0.000000	0.419420	H_o is rejected and H_a is accepted
PEU4	0.000001	0.675958	H_o is rejected and H_a is accepted
PEU5	0.000003	0.700242	H_o is rejected and H_a is accepted
TA1	0.000039	0.774270	H_o is rejected and H_a is accepted
TA2	0.000291	0.823952	H_o is rejected and H_a is accepted
SDR1	0.000000	0.540890	H_o is rejected and H_a is accepted
SDR2	0.000000	0.568295	H_o is rejected and H_a is accepted
SDR3	0.000000	0.360625	H_o is rejected and H_a is accepted
ADS1	0.000000	0.432532	H_o is rejected and H_a is accepted
ADS2	0.000000	0.188293	H_o is rejected and H_a is accepted
ADS3	0.000000	0.432532	H_o is rejected and H_a is accepted
IU1	0.000000	0.365679	H_o is rejected and H_a is accepted
IU2	0.000000	0.365679	H_o is rejected and H_a is accepted

Table 6 shows that the null hypothesis (H_0) is rejected, indicating that the data collected from the administered survey do not follow a normal distribution. Since the study involves ordinal qualitative variables, the Wilcoxon Signed-Rank Test (Wilcoxon, 1945) was used to test whether the median of the variables is significantly greater than 3. The test statistic T is given by:

$$T_+ = \sum positive\ signed\ ranks \tag{3}$$

$$T_- = \sum negative\ signed\ ranks \tag{4}$$

$$T = \min(T_+, T_-) \tag{5}$$

The test hypotheses are:

H_o: The median acceptance is ≤ 3
H_a: The median acceptance is > 3

The test statistic T was obtained using the statistical library from the Scipy Application Programming Interface (API) (Gommers et al., 2024), within the Jupyter Notebook development environment (Jupyter, 2025). The significance level used was α = 0.001. Table 7 shows the statistical results for each of the survey items.

Table 7. Results of the Wilcoxon Signed-Rank Test

Items	p-value	*T* test statistic	Conclusion (p < 0.001)
PU1	0.000000	351.0	H_o is rejected and H_a is accepted
PU2	0.000000	378.0	H_o is rejected and H_a is accepted
PU3	0.000000	406.0	H_o is rejected and H_a is accepted
PU4	0.000016	208.0	H_o is rejected and H_a is accepted
PEU1	0.000001	325.0	H_o is rejected and H_a is accepted
PEU2	0.000001	348.0	H_o is rejected and H_a is accepted
PEU3	0.000000	406.0	H_o is rejected and H_a is accepted
PEU4	0.000002	325.0	H_o is rejected and H_a is accepted
PEU5	0.000003	346.0	H_o is rejected and H_a is accepted
TA1	0.000005	300.0	H_o is rejected and H_a is accepted
TA2	0.000013	292.5	H_o is rejected and H_a is accepted
SDR1	0.000000	406.0	H_o is rejected and H_a is accepted
SDR2	0.000000	406.0	H_o is rejected and H_a is accepted
SDR3	0.000000	406.0	H_o is rejected and H_a is accepted
ADS1	0.000000	378.0	H_o is rejected and H_a is accepted
ADS2	0.000000	378.0	H_o is rejected and H_a is accepted
ADS3	0.000000	378.0	H_o is rejected and H_a is accepted
IU1	0.000000	378.0	H_o is rejected and H_a is accepted
IU2	0.000000	378.0	H_o is rejected and H_a is accepted

Table 7 shows that the null hypothesis (H_o) is rejected, providing extremely strong statistical evidence (due to the significance level) that learners perceive usefulness, ease of use, technology application, support digital resources, acquired digital skills, and intention to use above the neutral point. In other words, the remote laboratory is significantly accepted by the learners.

4 Conclusions

This paper presented the development and implementation of a technological environment using an RL in the area of Digital Logic Design, applying the V-model methodology for embedded systems. This technological environment enable remote manipulation and interaction of FPGA-based development platforms, offering an alternative to traditional in-person laboratories.

To support learner engagement and facilitate experimentation, nine lab exercises were specifically designed. These exercises reinforce theoretical content through a constructivist and connectivist learning approach, enabled by the proposed technological environment.

To evaluate the learners' acceptance of the RL, the TAM was applied using a data collection instrument based on a Likert-scale survey. The survey included six variables: PU, PEU, TA, SDR, ADS, and IU. The instrument's reliability was confirmed by a Cronbach's Alpha Coefficient of 0.866.

Descriptive statistical analysis showed that the sample mean ($\bar{x}$) across all survey items exceeded 4.14, indicating a high level of positive perception among learners. The coefficient of variation (CV), ranging between 8% and 18%, reflected strong to moderate homogeneity across the TAM variables.

Additionally, the Wilcoxon Signed-Rank Test provided extremely strong statistical evidence to reject the null hypothesis, confirming that learners agreed or strongly agreed with the usefulness and effectiveness of the proposed RL-based technological environment.

Finally, the evolution of I4.0 has introduced a wide range of emerging technologies that can be applied to education to improve teaching and learning processes. The E4.0 paradigm can be implemented through E-learning and B-learning approaches in different courses across all educational levels. One effective strategy involves the development of applications using the IoT technological environment with SoC platforms, which facilitate the deployment of RLs with low cost, high efficiency technologies, and wide applicability across disciplines.

Acknowledgments

The authors acknowledge the support provided by the National Autonomous University of Mexico (UNAM) and the National Polytechnic Institute (IPN), Mexico. They also acknowledge the support provided by the General Directorate for Academic Personnel Affairs (DGAPA-UNAM) through project IT400222, which is part of the Support Program for Research and Technological Innovation Projects (PAPIIT-UNAM). Additional support was received from the Secretariat for Research and Graduate Studies (SIP-IPN) through the Multidisciplinary Project (SIP registration number: 20240533) and the Innovation Project (SIP registration number: 20231117).
Finally, the authors express their gratitude to the National Council of Humanities, Sciences and Technologies (CONAHCyT) for the national postgraduate scholarship.

References

Álvarez Ariza, J. Á., & González Gil, S. (2022). RaspyLab: A low-cost remote laboratory to learn programming and physical computing through Python and Raspberry Pi. *IEEE Revista Iberoamericana de Tecnologías del Aprendizaje, 17*(2), 140–149. https://doi.org/10.1109/RITA.2022.3166877

AMD. (2025). *Vivado Design Suite User Guide: Using the Vivado IDE* (UG893). Retrieved June 15, 2025, from https://docs.amd.com/r/en-US/ug893-vivado-ide/Using-the-Vivado-IDE

Asociación de Internet MX. (2024). 20º Estudio sobre los hábitos de usuarios de internet en México. Retrieved March 15, 2025, from https://irp.cdn-website.com/81280eda/files/uploaded/20_Ha-bitos_de_Usuarios_de_Internet_en_Mexico_2024_VP.pdf

Booch, G., Jacobson, I., & Rumbaugh, J. (1996). The unified modeling language. *Unix Review*, *14*(13), 5.

Brown, C. E. (1998). Coefficient of variation. In *Applied multivariate statistics in geohydrology and related sciences* (pp. 155-157). Berlin, Heidelberg: Springer Berlin Heidelberg.

Butt, R., Siddiqui, H., Soomro, R. A., & Asad, M. M. (2020). Integration of Industrial Revolution 4.0 and IoTs in academia: A state-of-the-art review on the concept of Education 4.0 in Pakistan. *Interactive Technology and Smart Education, 17*(4), 337–354. https://doi.org/10.1108/ITSE-02-2020-0022

Chevalier, A., Copot, C., Ionescu, C. M., & De Keyser, R. (2016). A three-year feedback study of a remote laboratory used in control engineering studies. *IEEE Transactions on Education, 60*(2), 127–133. https://doi.org/10.1109/TE.2016.2605080

Cronbach, L. J. (1951). Coefficient alpha and the internal structure of tests. *Psychometrika*, *16*(3), 297-334.

Davis, F. D. (1989). Perceived usefulness, perceived ease of use, and user acceptance of information technology. *MIS Quarterly, 13*(3), 319–340. https://doi.org/10.2307/249008

Digilent Inc. (2025). *Nexys4 DDR™ FPGA Reference Manual*. Retrieved March 15, 2025, from https://digilent.com/reference/programmable-logic/nexys-4-ddr/reference-manual

Downes, S. (2022). Connectivism. *Asian Journal of Distance Education, 17*(1), 58–87. https://doi.org/10.5281/zenodo.6173510

Flores Olvera, D.M., Guzmán Games, F.J., Martínez Barragán, Y.M., Ibarra Cruz, E., & Alvear Cortés, E. (2020). Educación 4.0, origen para su fundamentación. *Contribuciones de la tecnología digital en el desarrollo educativo y social*, 165-177. Eindhoven, NL: Adaya Press.

Fujieda, N., & Okuchi, A. (2023, November). A novel remote FPGA lab platform using MCU-based controller board. In *Proceedings of the 2023 IEEE International Conference on Teaching, Assessment and Learning for Engineering (TALE)* (pp. 1–6). IEEE.

Fundación México-Estados Unidos para la Ciencia (FUMEC). (2022). *FUMEC a 30 años de su creación*. Retrieved March 15, 2025, from https://www.fumec.org/Publicaciones

Gommers, R., Virtanen, P., Haberland, M., Burovski, E., Reddy, T., Weckesser, W., Striega, K. (2024). *scipy/scipy: SciPy 1.15.0* [Software]. Zenodo.

IEEE. (2019). *IEEE standard for VHDL language reference manual (IEEE Std 1076-2019)* (pp. 1–673). https://doi.org/10.1109/IEEESTD.2019.8938196

Instituto Nacional de Estadística y Geografía (INEGI). (2024). *Encuesta Nacional sobre Disponibilidad y Uso de Tecnologías de la Información en los Hogares (ENDUTIH)*. Recuperado el 15 de marzo de 2025, de https://www.inegi.org.mx/programas/endutih/2024/

Ishak, R., & Mansor, M. (2020). The relationship between knowledge management and organizational learning with academic staff readiness for education 4.0. *Eurasian Journal Education*. 85, 169–184.

Jalilibal, Z., Amiri, A., Castagliola, P., & Khoo, M. B. (2021). Monitoring the coefficient of variation: A literature review. *Computers & Industrial Engineering, 161*, 107600. https://doi.org/10.1016/j.cie.2021.107600

Kramp, T., Van Kranenburg, R., & Lange, S. (2013). Introduction to the Internet of Things. In *Enabling things to talk: Designing IoT solutions with the IoT architectural reference model* (pp. 1-10). Berlin, Heidelberg: Springer Berlin Heidelberg.

Kumar, S., Tiwari, P., & Zymbler, M. (2019). Internet of Things is a revolutionary approach for future technology enhancement: A review. *Journal of Big Data, 6*(1), 1–21. https://doi.org/10.1186/s40537-019-0269-8

Melosik, M., Naumowicz, M., Kropidłowski, M., & Marszalek, W. (2022). Remote prototyping of FPGA-based devices in the IoT concept during the COVID-19 pandemic. *Electronics, 11*(9), 1497. https://doi.org/10.3390/electronics11091497

Milenkovic, M. (2020). *Internet of Things: Concepts and System Design*. Springer Nature.

MIPI Alliance. (n.d.). *MIPI CSI-2® specification*. Retrieved March 15, 2025, from https://www.mipi.org/specifications/csi-2

Mourtzis, D., Vlachou, E., Dimitrakopoulos, G., & Zogopoulos, V. (2018). Cyber-physical systems and education 4.0: The teaching factory 4.0 concept. *Procedia Manufacturing, 23*, 129–134. https://doi.org/10.1016/j.promfg.2018.04.005

Mukul, E., & Büyüközkan, G. (2023). Digital transformation in education: A systematic review of education 4.0. *Technological Forecasting and Social Change, 194*, 122664. https://doi.org/10.1016/j.techfore.2023.122664

Naciones Unidas. (2018). *La Agenda 2030 y los Objetivos de Desarrollo Sostenible: Una oportunidad para América Latina y el Caribe* (LC/G.2681-P/Rev.3). Santiago de Chile: CEPAL.

Navas-González, R., Oballe-Peinado, Ó., Castellanos-Ramos, J., Rosas-Cervantes, D., & Sánchez-Durán, J. A. (2023). Practice projects for an FPGA-based remote laboratory to teach and learn digital electronics. *Information, 14*(10), 558. https://doi.org/10.3390/info14100558

Núñez-Barriopedro, E., Monclúz, I. M., & Ravina-Ripoll, R. (2019). El impacto de la utilización de la modalidad B-learning en la educación superior. *Alteridad. Revista de Educación, 14*(1), 26–39. https://doi.org/10.17163/alt.v14n1.2019.02

Oviedo, H. C., & Campo-Arias, A. (2005). Aproximación al uso del coeficiente alfa de Cronbach. *Revista Colombiana de Psiquiatría, 34*(4), 572–580.

Pandas development team. (n.d.). *User guide*. Retrieved June 15, 2025, from https://pandas.pydata.org/docs/user_guide/index.html

Project Jupyter. (n.d.). *Project Jupyter documentation*. Retrieved June 15, 2025, from https://docs.jupyter.org/en/latest/

Puncreobutr, R. (2016). Education 4.0: New challenge of learning. *St. Theresa Journal of Humanities and Social Sciences, 2*(2), 92–97.

Raspberry Pi Ltd. (2025). *Raspberry Pi Camera Module 2*. Retrieved March 15, 2025, from https://www.raspberrypi.com/products/camera-module-v2/

Raspberry Pi Ltd. (2025b). *Raspberry Pi 4 Model B: Product brief*. Retrieved March 15, 2025, from https://datasheets.raspberrypi.com/rpi4/raspberry-pi-4-product-brief.pdf

Raspberry Pi Ltd. (2025c). *Operating system images*. Retrieved March 15, 2025, from https://www.raspberrypi.com/software/operating-systems/

Ríos, A. R., & Peña, A. M. P. (2020). Estadística inferencial. Elección de una prueba estadística no paramétrica en investigación científica. *Horizonte de la Ciencia*, *10*(19), 191-208.

Schwab, K. (2016). *La cuarta revolución industrial*. Ginebra, Suiza: World Economic Forum.

Shapiro, S. S., & Wilk, M. B. (1965). An analysis of variance test for normality (complete samples). *Biometrika, 52*(3–4), 591–611.

Siemens, G. (2005). Connectivism: A learning theory for the digital age. *International Journal of Instructional Technology and Distance Learning*. Retrieved March 15, 2025, from http://www.itdl.org/Journal/Jan_05/article01.htm

Sony. (2025). IMX219PQH5-C. Retrieved March 15, 2025, from https://github.com/rellimmot/Sony-IMX219-Raspberry-Pi-V2-CMOS.

Streiner, D. L. (2003). Starting at the beginning: An introduction to coefficient alpha and internal consistency. *Journal of Personality Assessment, 80*(1), 99–103. https://doi.org/10.1207/S15327752JPA8001_18

Trilla, J., & García Carrasco, E. (2001). *El legado pedagógico del siglo XX para la escuela del siglo XXI* (Vol. 241). Barcelona, España: Graó.

United Nations Department of Economic and Social Affairs. (2023). *Informe de los Objetivos de Desarrollo Sostenible 2023: Edición especial*. Naciones Unidas. https://unstats.un.org/sdgs/report/2023/The-Sustainable-Development-Goals-Report-2023_Spanish.pdf

Van Dijk, J. (2020). *The digital divide*. John Wiley & Sons.

Vargas, G. A. T., & Durá Martínez, R. A. (2014). El cómputo ubicuo y su importancia para la construcción del internet de las cosas y el big data. *Revista General de Información y Documentación, 24*(2), 217–232. https://doi.org/10.5209/rev_RGID.2014.v24.n2.47491

Wilcoxon, F. (1945). Individual comparisons by ranking methods. *Biometrics Bulletin, 1*(6), 80–83. https://doi.org/10.2307/3001968

Xilinx Inc. (n.d.). *7 series product selection guide: Artix-7 FPGAs*. Retrieved March 15, 2025, from https://docs.amd.com/v/u/en-US/7-series-product-selection-guide